Uniplanar Monolithic Frequency Doublers

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Abstract — **GaAs monolithic frequency doublers in the 13 GHz band and 26 GHz band have been designed and fabricated. These doublers employ a newly developed uniplanar monolithic microwave IC (MMIC) structure. They are composed of coplanar waveguides, slotlines, and air bridges only on the upper side of the GaAs substrate. These uniplanar MMIC frequency doublers offer the advantages of smaller circuit size and simpler fabrication processes than microstrip-based MMIC's. The fabricated doublers have achieved a conversion gain of 2.9 dB at 12.4 GHz and a minimum conversion loss of 0.7 dB at 24.4 GHz. Furthermore, a 6.5 GHz to 26 GHz frequency quadrupler has been made using a cascade connection of the doubler chips. It demonstrated stable operation without any adjustment and achieved a conversion loss of 10 dB.**

I. Introduction

AS A FREQUENCY multiplying device, a GaAs MESFET has the advantages of input–output isolation and possible conversion gain and is suitable for monolithic integration. Doubling characteristics of FET's have been studied theoretically [1], [2] and experimentally [3], [4], and several FET doublers using hybrid [2], [5], [6] or monolithic [7] integration techniques have been reported.

Monolithic microwave integrated circuit (MMIC) technology is attractive because it can reduce the size and cost of microwave circuits. The circuit size of the reported doublers, however, is rather large since a frequency doubler requires a quarter-wavelength fundamental frequency trap or large hybrid circuits for a balanced operation. It causes the fabrication cost to increase and makes larger scale monolithic integration difficult. Therefore, size reduction of the passive portion in the MMIC has been required.

In this paper, a balanced monolithic frequency doubler circuit using a "uniplanar" MMIC structure [8] is proposed. A uniplanar MMIC employs coplanar waveguides, a slotline, and air bridges on the upper side of the semiconductor substrate. It has the advantages of (1) easy antiphase signal division using slotlines, (2) good grounding without via holes, and (3) on-wafer circuit testing. These advantages have been demonstrated in various junctions, transitions, and hybrid circuits [8]. This paper shows applications of this structure to active FET circuits. The antiphase excitation of FET's required for balanced operation is also carried out using a simple uniplanar circuit configuration. The uniplanar balanced frequency doublers proposed here have the features of (1) wide-band fundamental frequency suppression owing to the balanced configuration and (2) small circuit size due to the elimination of the quarter-wavelength fundamental frequency trap or hybrid circuits required in conventional balanced doublers.

The uniplanar frequency doublers were designed and fabricated to have output frequencies of 13 GHz and 26 GHz and they exhibited good performance. A maximum conversion gain of 2.9 dB has been obtained at an output frequency of 12.4 GHz with an input power of 5 dBm, and a minimum conversion loss of 0.7 dB was obtained at an output frequency of 24.4 GHz and an input power of 5 dBm. The 13 GHz and 26 GHz doublers were directly connected and showed stable quadrupling characteristics.

Manuscript received December 29, 1988; revised March 23, 1989.

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IEEE Log Number 8928334.

II. Uniplanar Balanced Circuit

A quarter-wavelength open-circuited stub is often used in single-ended frequency doublers in order to suppress the fundamental frequency component [7]. It is too large, however, to be included on a small MMIC, because a quarter wavelength at, for example, 6 GHz is longer than 4 mm on a GaAs substrate. In a balanced frequency doubler, this kind of a stub circuit is not required. However, a large balun circuit or hybrid circuit is needed if the doubler is designed using microstrip lines [6]. Since circuit size is a great factor affecting IC cost, it represents a major obstacle to the development of a low-cost MMIC frequency doubler.

The uniplanar configuration shown in Fig. 1 presents a way to overcome this problem. The input signal fed from the coplanar waveguide in Fig. 1 passes through a coplanar waveguide/slotline transition. It propagates on the slotline and excites two FET's in antiphase through a matching circuit. Second-harmonic signals generated by the FET nonlinearity near pinch-off are combined in phase at a junction in the output circuit and obtained from a coplanar waveguide. On the other hand, fundamental frequency components appearing in antiphase at the drain are canceled and reflected at the junction. This circuit needs no "quarter-wavelength" element. Therefore, it can be made smaller if a compact coplanar waveguide/slotline transition [8] is employed.

III. Circuit Design

A. Consideration of Operating Point and Load Conditions

FET doublers can be classified into two groups. One operates at a gate–source voltage near pinch-off, the other at nearly zero voltage. There is no large difference in

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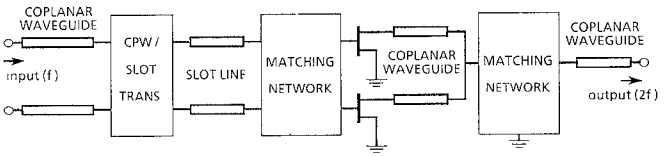


Fig. 1. Circuit configuration of a uniplanar balanced frequency doubler.

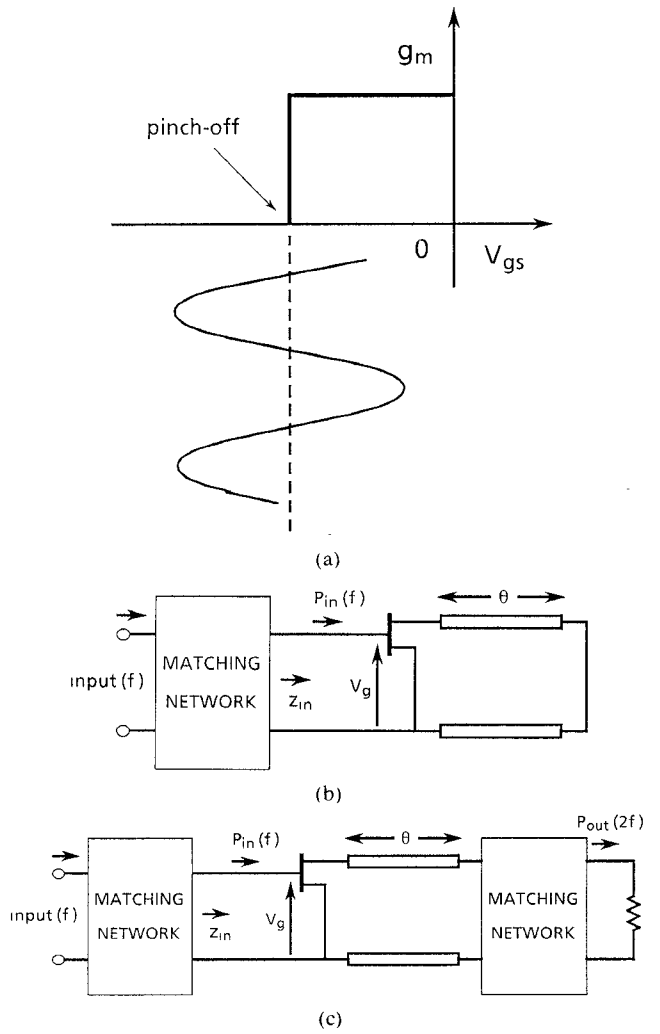


Fig. 2. Simplified doubler model. (a) Transconductance model. (b) Equivalent circuit for fundamental frequency component. (c) Equivalent circuit for second harmonic frequency component.

conversion gain or loss between these two groups because the largest contribution to second-harmonic generation is from the drain current clipping effect [1]. "Pinch-off" doublers, however, have lower power consumption and are free of large gate current. The type which operates near pinch-off is selected for these reasons.

Another basic and important design item concerns load conditions. Since the fundamental frequency component appearing at the drain is reflected at the junction in the doubler's output circuit as shown in Fig. 2, the electrical length between the FET drain and the junction largely affects conversion efficiency [2]. In order to determine this

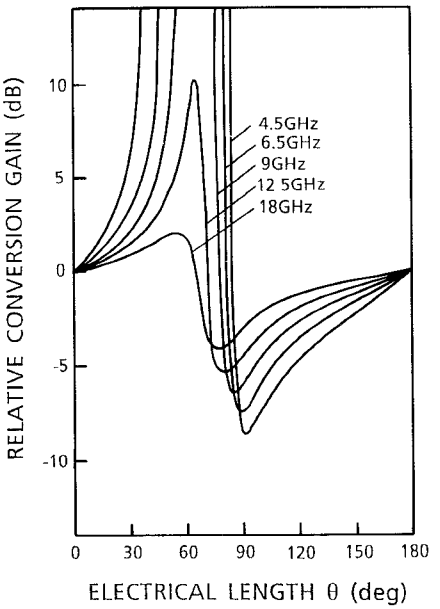


Fig. 3. Relative conversion gain as a function of electrical length θ between FET drains and the junction.

length, a simplified estimation was performed using the linear circuit model shown in Fig. 2.

The second-harmonic output power $P_{out}(2f)$ is proportional to the square of the drain current second-harmonic component $|I_d(2f)|$. If a simple transconductance model as shown in Fig. 2(a) is assumed, $|I_d(2f)|$ is proportional to the drain current fundamental component $|I_d(f)|$. Therefore, the relative conversion gain G_c can be written as

$$G_c = \frac{|I_d(f)|^2}{P_{in}(f)} = \frac{g_m^2 \cdot |V_g(f)|^2}{4P_{in}(f)} = \frac{g_m^2}{4} \cdot \frac{|Z_{in}|^2}{R_{in}} \quad (1)$$

where $P_{in}(f)$ is the input power, $V_g(f)$ is the fundamental frequency component of the gate voltage, Z_{in} is the input impedance, and R_{in} is the real part of Z_{in}. From this formula, the effect of the length θ in Fig. 2 can be roughly estimated by calculating the input impedance of the circuit in Fig. 2(b). Resultant relative conversion gain curves against electrical length θ of the line are shown in Fig. 3 for a FET with 100 μm gate width. The calculated gain values are normalized by the value at $\theta = 0$. The input impedance of the FET is shown in Fig. 4. The real part of the input impedance R_{in} decreases as the electrical length θ increases from zero. This means that a larger electrical length θ offers higher conversion efficiency. However, this also leads to difficulty in broad-band matching.

The bandwidth of the input matching network is also estimated. If the simple matching network illustrated in Fig. 5(a) is assumed, the inductance L and capacitance C for the complete match at center frequency ω_0 must be

$$L = -X_{in}/\omega_0 + [R_{in}(1-R_{in})]^{1/2}/\omega_0 \quad (2)$$

$$C = [(1-R_{in})/R_{in}]^{1/2}/\omega_0 \quad (3)$$

where L, C, R_{in}, and X_{in} are normalized by the standard impedance. The bandwidth of 10 dB return loss or more of

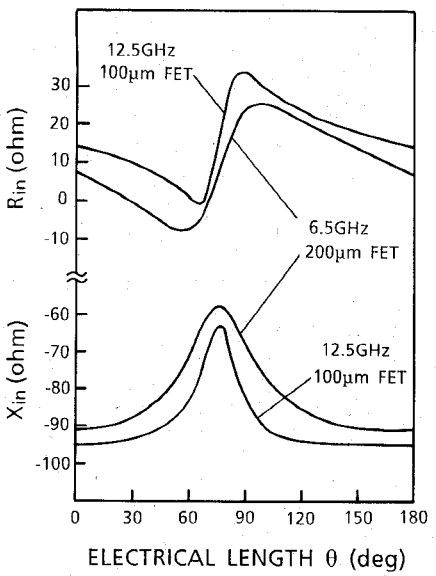
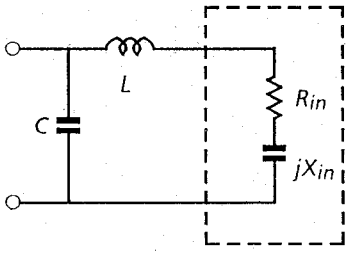
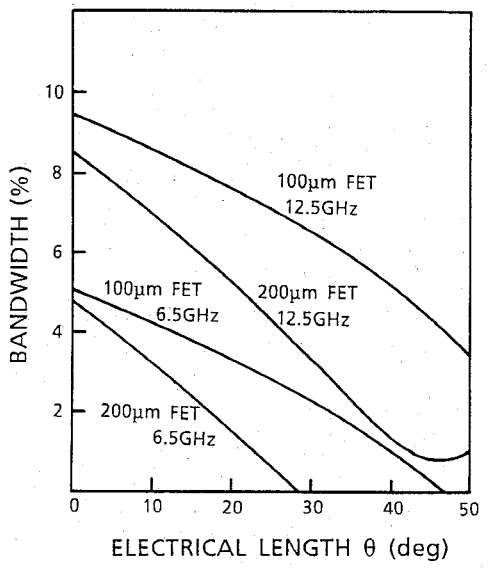


Fig. 4. Input impedance as a function of electrical length θ between FET drains and the junction.



(a)



(b)

Fig. 5. Effect of electrical length θ on input matching network bandwidth. (a) Assumed input matching network. (b) Input matching network bandwidth as a function of electrical length θ between FET drains and the junction.

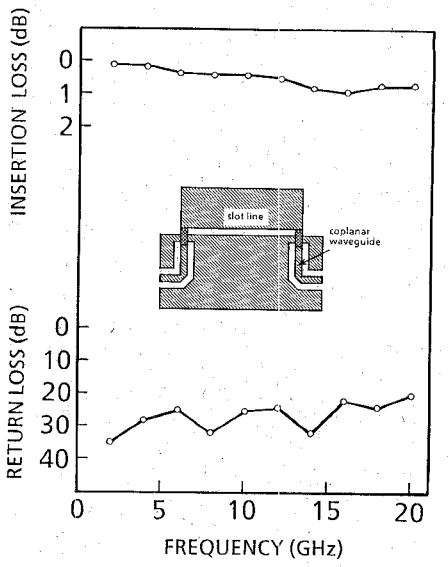


Fig. 6. Transmission and reflection characteristics of coplanar waveguide/slotline transition.

this matching network is plotted in Fig. 5(b). It can be seen that a long θ results in a narrow bandwidth.

Therefore, the distance between FET drains and the junction is chosen to be rather short for wide-band operation and small circuit size. This is favored over the highest conversion gain.

B. Matching Network

The time-domain circuit simulator SPICE was used in the process of designing the matching network in order to investigate the large-signal input impedance of the FET with the load condition discussed above, operating near pinch-off. The gate-to-source voltage waveform and current waveform were first obtained through transient analysis. Next, fundamental frequency components were extracted by Fourier analysis and the input impedance was calculated. The FET model used here is a modified JFET model which has an additional "channel thickness modulation" parameter γ [9].

Matching networks can be constructed using spiral inductors of small size and metal–insulator–metal (MIM) capacitors. Two terminals of the slotline end are connected to the FET gates by these spiral inductors. Air bridges are used at the coplanar waveguide discontinuities in order to equalize the potentials of the two ground planes. The bias voltage for the FET gate is supplied simply through decoupling resistors.

C. Coplanar Waveguide/Slotline Transition

The transmission and reflection characteristics of the coplanar waveguide/slotline transition obtained through test circuit measurements are shown in Fig. 6. The slotline length in the test circuit is 500 μm. The return loss is larger than 25 dB at frequencies below 15 GHz. This performance is good enough for doubler applications.

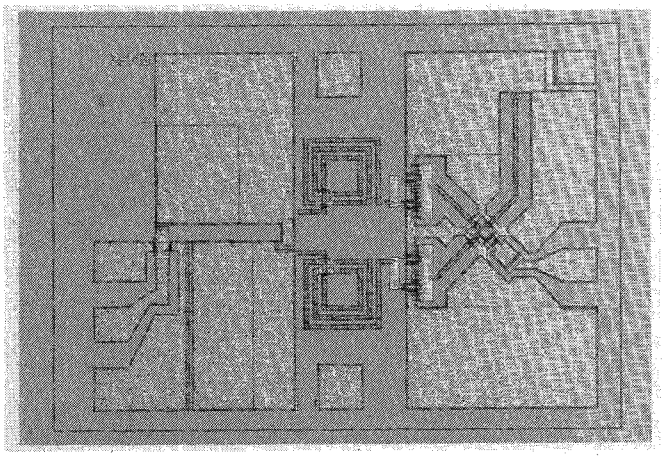


Fig. 7. 13 GHz to 26 GHz frequency doubler chip.

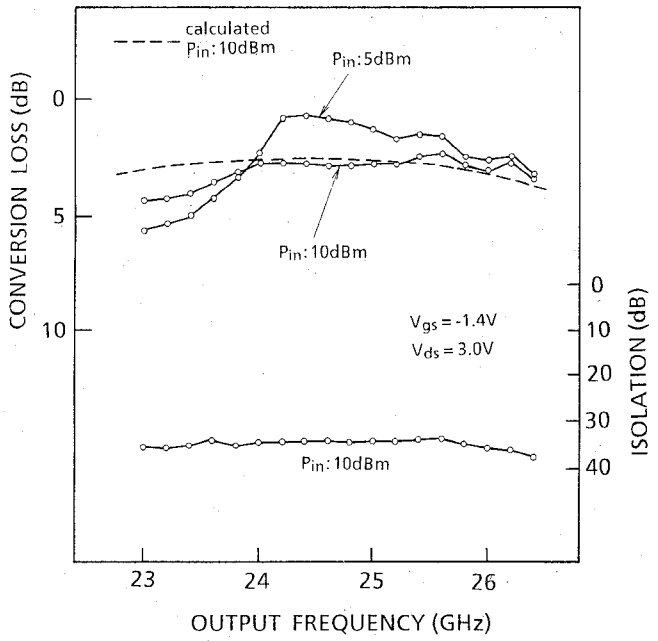


Fig. 8. Conversion loss of the 13 GHz to 26 GHz frequency doubler.

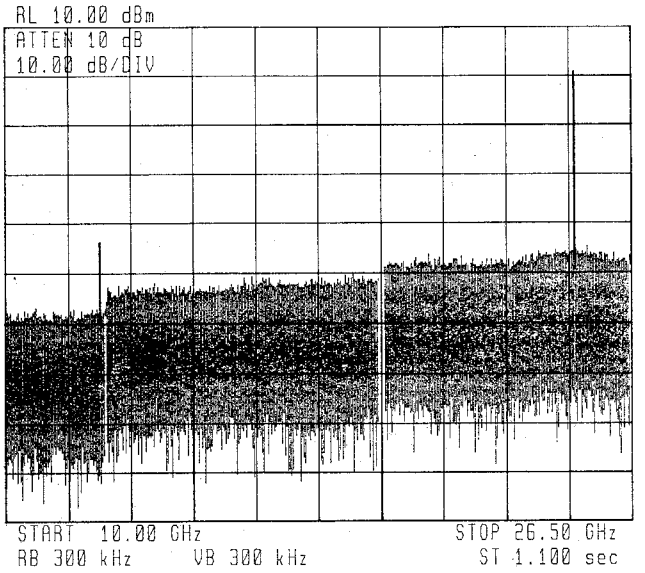


Fig. 9. Output spectrum of the 13 GHz to 26 GHz frequency doubler (V: 10 dB/div, H: 1.65 GHz/div, 10 GHz–26.5 GHz).

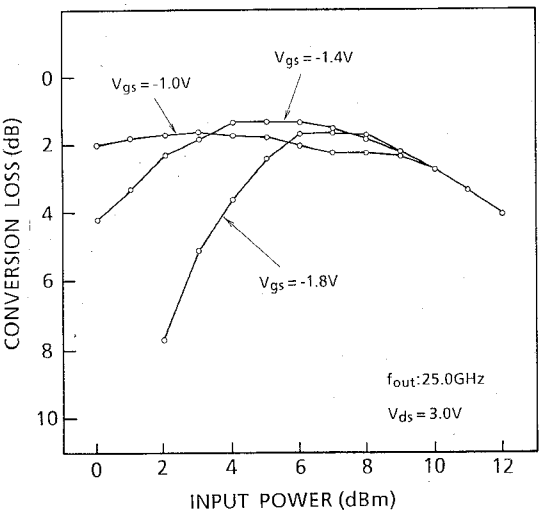


Fig. 10. Dependence of conversion loss on input power level at the center frequency.

IV. Performance of Monolithic Frequency Doublers

A. 13 GHz to 26 GHz Frequency Doubler

The 26 GHz uniplanar frequency doubler was fabricated on a 600-μm-thick GaAs substrate using the process called advanced SAINT [10]. The doubler chip is shown in Fig. 7. The input matching network at 13 GHz consists of spiral inductors and MIM capacitors. In the 26 GHz output circuit, high-impedance (75 Ω) coplanar waveguides are employed in order to reduce the line length. The distance between FET drains and the junction in the output circuit is about 120 μm. This corresponds to an electrical length θ of 4.5°. The gate widths of the two FET's are 100 μm.

The measured frequency response is shown in Fig. 8 with calculated values at input powers of 5 dBm and 10 dBm. Conversion loss was lower than 4 dB in the wide frequency range of 23.7 GHz to 26.5 GHz with an input power of 10 dBm. The minimum conversion loss for the 5 dBm power input was 0.7 dB. In calculation, a time-domain circuit simulation using SPICE was performed, and the second-harmonic component was extracted from the output voltage waveforms. The fundamental frequency component measured at the output was 30 dB lower than the desired second-harmonic component. This wide-band suppression is one of the advantages of the uniplanar balanced configuration. Fig. 9 shows an output spectrum. The converted signal and the suppressed fundamental signal can be seen.

Conversion loss as a function of input power at the center frequency is shown in Fig. 10. It can be seen that the optimum gate bias voltage shifts to a lower level as input power increases. Conversion loss at a band edge is shown in Fig. 11. Conversion efficiency reaches a maximum at a higher input power level in Fig. 11 than in Fig. 10. Since the input matching at a band edge is not as good

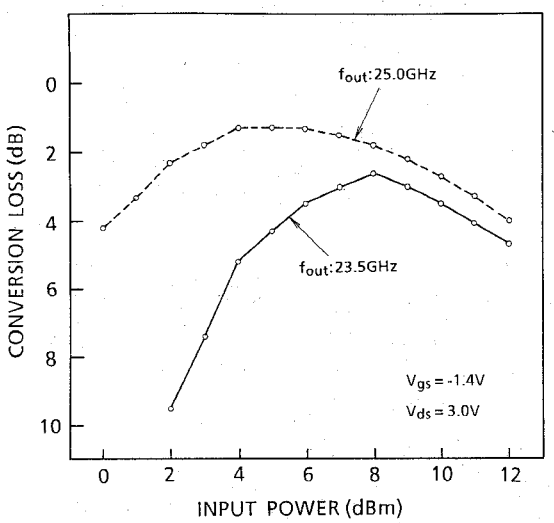


Fig. 11. Dependence of conversion loss on input power level at a band edge.

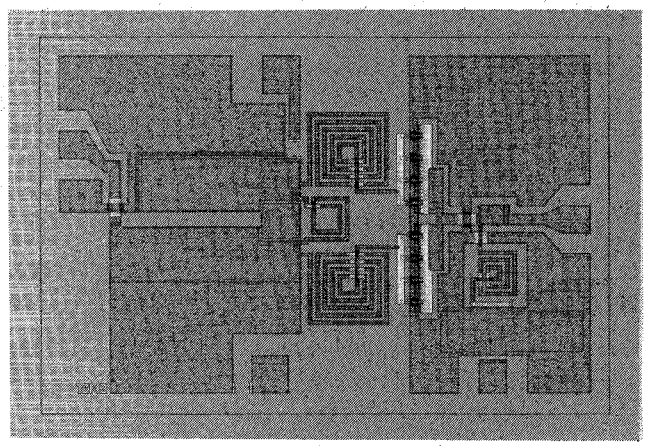


Fig. 12. 6.5 GHz to 13 GHz frequency doubler chip.

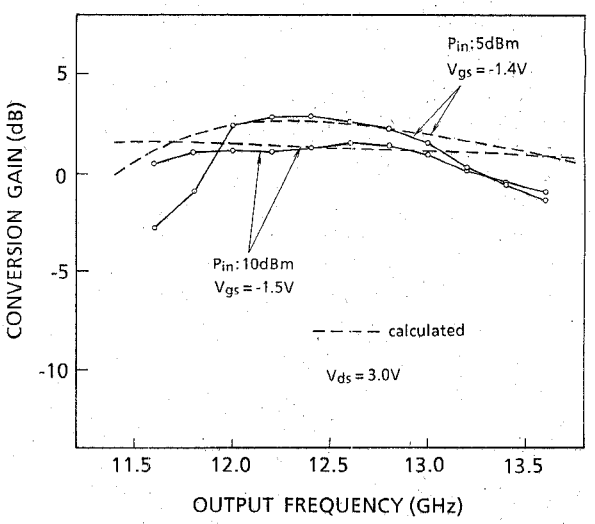


Fig. 13. Conversion gain of the 6.5 GHz to 13 GHz frequency doubler.

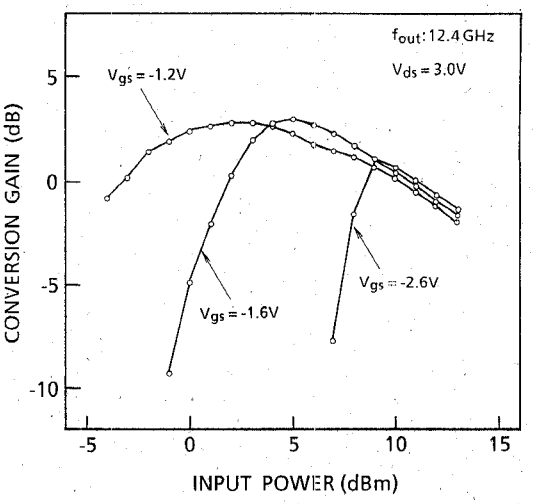


Fig. 14. Dependence of conversion gain on input power level.

as that at the center frequency, increasing the input power provides the optimum input level at the FET's, as can be seen in Fig. 11. At a higher input power level, the power fed to the FET's is optimum at the band edge, and it is too high at the center frequency. This is because higher input power results in flat frequency response and broader bandwidth, as shown in Fig. 8. The circuit size is only 1.3×0.9 mm^2, owing to the novel uniplanar configuration and the lumped-constant matching network. This circuit size is much smaller than that of the microstrip-based doubler, 3×2 mm^2 [7].

B. 6.5 GHz to 13 GHz Frequency Doubler

A 13 GHz doubler chip, shown in Fig. 12, was fabricated using the same process as for the 25 GHz doubler. The distance between FET drains and the junction in the output circuit was selected to be zero for the reason discussed in subsection III-A. The FET's have gate widths of 200 μm. The measured frequency response is shown in Fig. 13. When the input power was 10 dBm, the conversion gain was observed at the output frequencies from 11.5 GHz to 13.2 GHz. The maximum conversion gain obtained was 2.9 dB at 12.4 GHz with a 5 dBm input. The dependence of the conversion gain on the input power level is shown in Fig. 14. Power consumption was 75 mW at the center frequency with a 10 dBm signal power input. The circuit size is 1.0×1.5 mm^2.

C. 6.5 GHz to 26 GHz Cascade Operation

A frequency quadrupler module was assembled using a direct connection of the 13 GHz and 26 GHz doubler chips. The chips were tested on a wafer in advance. Since the first stage doubler had 0 dB conversion loss performance, no interstage amplifier was necessary. Additional transmission lines of 10 mm in total and coaxial test connectors were used with the directly connected doubler chips. The assembled frequency quadrupler module showed stable quadrupler performance. The conversion loss was about 10 dB at the center frequency with a 10 dBm power input as shown in Fig. 15, which includes connection loss and the loss of the additional lines in the test fixture. The total power consumption was 130 mW.

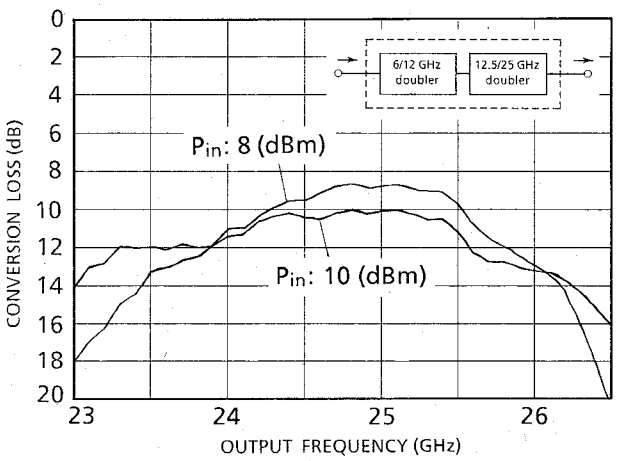


Fig. 15. Frequency quadrupler performance of cascaded frequency doublers.

V. Conclusion

A uniplanar MMIC structure was successfully applied to balanced frequency doublers. The doubler circuits consist of coplanar waveguides and a slotline. Consequently, they have a ground plane on the upper side of the substrate. Therefore, good grounding without via holes and on-wafer measurement by the use of microwave wafer probes are possible. First, balanced monolithic doublers were designed for use in the 13 GHz and 26 GHz bands and fabricated on GaAs substrates using the advanced SAINT process. They showed good performance and their circuitry was small. Second, the 13 GHz and 26 GHz doublers were connected in cascade and good experimental results were obtained. The uniplanar MMIC technology has the advantage of small circuitry, and it allows the integration of many functions on a single MMIC chip.

Acknowledgment

The authors wish to thank Dr. T. Sugeta, Dr. O. Kurita, Dr. K. Yamamoto, and Dr. M. Muraguchi for their helpful advice and fruitful discussions, and M. Hirayama and Dr. K. Ohwada for their support in MMIC fabrication. They also thank Dr. K. Kohiyama and Dr. H. Yamamoto for their advice and encouragement.

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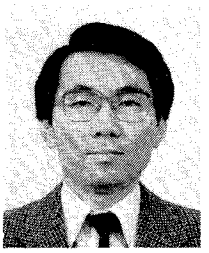

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